Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **+V SUPPLY**
2. **N/C**
3. **IN 16**
4. **IN 15**
5. **IN 14**
6. **IN 13**
7. **IN 12**
8. **IN 11**
9. **IN 10**
10. **IN 9**
11. **GND**
12. **V REF**
13. **ADDRESS A3**
14. **ADDRESS A2**
15. **ADDRESS A1**
16. **ADDRESS A0**
17. **ENABLE**
18. **IN 1**
19. **IN 2**
20. **IN 3**
21. **IN 4**
22. **IN 5**
23. **IN 6**
24. **IN 7**
25. **IN 8**
26. **–V SUPPLY**
27. **OUT**

**3**

**4**

**5**

**6**

**7**

**8**

**9**

**10**

**2 1 27 26**

**11 12 13 14 15 16 17**

**1690 1**

**MASK**

**REF**

**25**

**24**

**23**

**22**

**21**

**20**

**19**

**18**

**.084”**

**.159”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0036” X .0036”**

**Backside Potential: FLOATING or –Vsupply**

**Mask Ref: 1690 1**

**APPROVED BY: DK DIE SIZE .084” X .159” DATE: 8/25/21**

**MFG: HARRIS THICKNESS .019” P/N: HI0-506A**

**DG 10.1.2**

#### Rev B, 7/1